

A New Efficient Approach for Designing Intelligence Interleaver

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Abstract-In communication system for removing burst error various algorithms, techniques are used. This paper contains designing of interleaving based on Artificial Intelligence state space search technique i.e. Breadth first search (BFS) and Depth first search (DFS), which gives number of possible solution, from the number of solution designer choose best solution. This algorithm is totally different from traditional algorithm. This algorithm takes more time than conventional algorithm but designer obtained result which is more efficient as compared with traditional.

Index Terms-Interleaver, burst error, security, BFS, DFS, Artificial Intelligence, State space search, BER, FEC Codes, Noise.

1. INTRODUCTION

Currently all the fiber based interleavers are basically having two ports. For achieving the high channel counts for any Communication system number of interleaver are used. As increasing the number of interleavers, the insertion loss increases [1]. Optical interleavers are basically filters that separate an incoming signal's spectrum odd and even channels [2]. In today's scenario in field of Mobile communication during data transfer there are various types of error occurs i.e. due to noise. Noise may be internal or external. Internal noise generates inside the electronics system on other hand external noise is due to from outside source. In Analog Communication the performance of the system is measured in terms of SNR (Signal to Noise Ratio). In Digital Communication for improving performance of the system i.e. BER, Data transferring rate, security we apply several types of Forward Error Correcting Codes or in other word Source Coding and Channel Coding. Forward Error Correcting code is having very good advantage i.e. these codes can correct as well as detect the error. After applying various types of coding the performance of the communication system has been improved. As improving the performance of communication system in terms of BER there is another type of error occur i.e. Burst Error. When there is error in 2 or more than 2 continuous bit, this type of error can be termed as Burst Error. For removing this type of error researcher gave the idea of interleaving the data i.e. Interleaver. For removing burst error, we design a block that can termed as Interleaver. Interleaving can be applied in both wired and wireless communication. there was no such standard way for designing interleaver but during designing of interleaver designer must remember some key points that are interleaver must be design in such a way that deinterleaving designing be possible of

Interleaved data. In this work we will design interleaver based upon state space search based techniques i.e. BFS (Breadth First Search), Breadth first search is the prototype of many important graph algorithms such as minimum spanning tree algorithm: shortest path algorithm and so on, which are similar with breadth first sea& Furthermore it is one of the simplest searching algorithms in graph theory [5]. And DFS (Depth First Search). BFS has wide applications in EDA and also in other fields [8]. A block interleaver accepts a set of symbols and rearranges them, without repeating or omitting any of the symbols in the set. The number of symbols in each set is fixed for a given interleaver. The interleaver's operation on a set of symbols is independent of its operation on all other sets of symbols. An interleaver permutes symbols according to a mapping. A corresponding deinterleaver uses the inverse mapping to restore the original sequence of symbols. Interleaving and deinterleaving can be useful for reducing errors caused by burst errors in a communication system. A interleaver can be assumed a black box that takes input bits and gives interleaved bits which are shown in figure-1 given below.



Figure 1- Block Diagram of Interleaver

2. PREVIOUS WORK RELATED TO INTERLEAVER

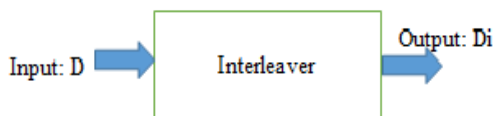
2.1 Interleaving of Random Data in Matrix Format

In this kind of designing, the data is taken in such a way that bits are mapped into square matrix. Considering 3X3 Matrices with 9 bit of random input data. $D = \{1,2,3,4,5,6,7,8,9\}$

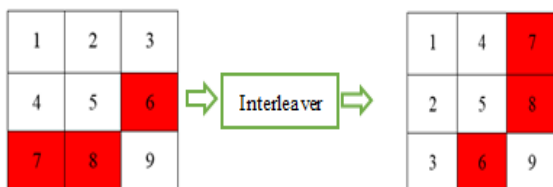
1	2	3
4	5	6
7	8	9

Let Error is in 6th, 7th and 8th position

1	2	3
4	5	6
7	8	9



Where D: Input Data, Di: Interleaved Data



- 1st format
 $Di(1) = \{1,4,7,8,5,2,3,6,9\}$ -----(1)
 In this case the 1 bit is safe from the burst error , but here there is also burst error.
- 2nd Format
 $Di(2) = \{1,2,4,3,5,7,6,8,9\}$ -----(2)
 In this case burst error is not removed.
- 3rd Format
 $Di(3)=\{1,4,7,8,9,6,3,2,5\}$ -----(3)

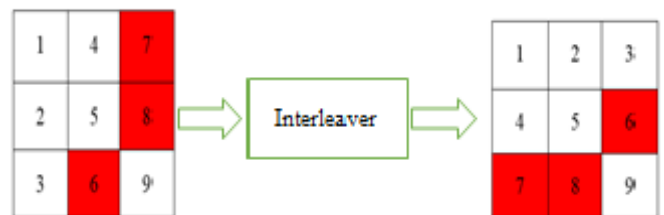
In this case there is also burst error present. Here burst error is partially removed.

2.2 Interleaving of Random Data in Reverse Matrix Format

Here in this kind of designing, the data is also taken in such a way that bits are mapped into square matrix. Here Data is same of 9-bit.
 $D = \{1,2,3,4,5,6,7,8,9\}$

1	4	7
2	5	8
3	6	9

Here the data is entered in other format. Here we are assuming the burst error 6th, 7th and 8th bit.



- 1st format
 $Di(1) = \{1,2,3,6,9,8,7,4,5\}$ -----(4)
 In this case the 1 bit is safe from the burst error , but here there is also burst error.
- 2nd Format
 $Di(2) = \{1,4,2,7,5,3,8,6,9\}$ -----(5)
 In this case burst error is not removed.
- 3rd Format
 $Di(3) = \{1,2,3,6,9,8,7,4,5\}$ -----(6)
 In this case there is also burst error present. Here burst error is partially removed.

2. STATE SPACE SEARCH TECHNIQUE BASED INTERLEAVING DESIGNING

State Space search technique is modern technique which is based upon Artificial Intelligence. It can be classified into two types 1. BFS, 2.DFS. Which are also given in figure-2.

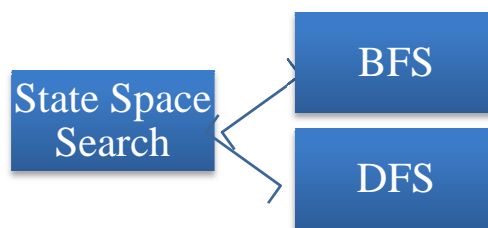


Figure 2- State Space Search Technique

2.1. First Approach MBAID (Map in BFS And Interleaved in DFS):

In this technique for designing the interleaver both techniques will be used. In this technique first map input bits in BFS and then Interleaved in DFS. Here we are considering 9- bit data. Data is random in nature.

$$D = \{1,2,3,4,5,6,7,8,9\} \text{-----(7)}$$

D: is Input bits

Steps:

- a. First Map the input bit in tree using BFS
- b. Now Interleave bits acc. to DFS
- c. Write the interleaved bits in BFS pattern
- d. Now analysis the result.

Note: Here also assuming same error bits 6th, 7th and 8th.

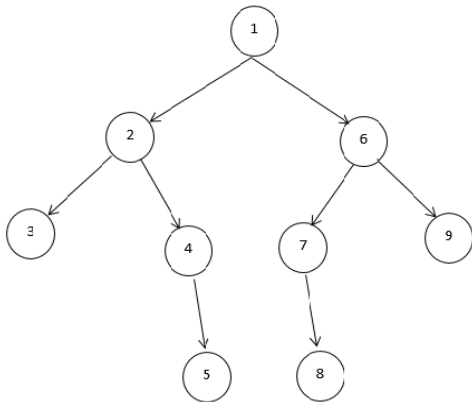


Figure 3- Input bits in BFS Pattern

Applying Interleaving on this BFS pattern and interleaved results in DFS Pattern.

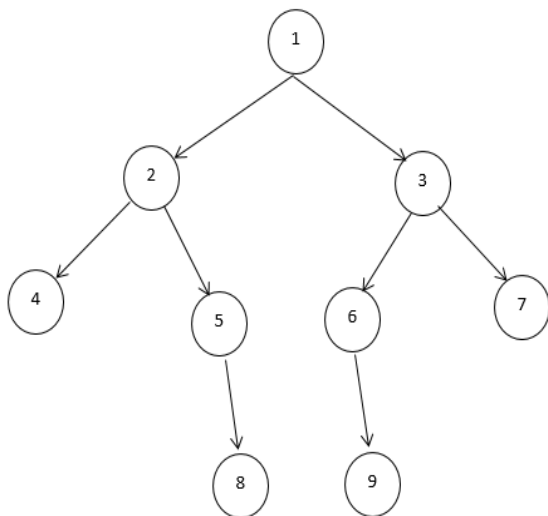


Figure 4- Interleaved DFS Pattern output

Output Interleaved bit

$$D_i = \{1,2,4,5,8,3,6,9,7\} \text{-----(8)}$$

From Equation 8 it is clear that the burst error is removed.

2.2. Second Approach MDAIB(Map in DFS And Interleaved in BFS):

Here in this technique also for designing the interleaver both techniques will be used. In this technique first map input bits in DFS and then Interleaved in BFS. Here we are considering 9- bit data.

$$D = \{1,2,3,4,5,6,7,8,9\} \text{-----(7)}$$

D: is Input bits

Steps:

- a. First Map the input bit in tree using DFS
- b. Now Interleave bits acc. to BFS
- c. Write the interleaved bits in DFS pattern
- d. Now analysis the result.

Note: Here also assuming same error bits 6th, 7th and 8th.

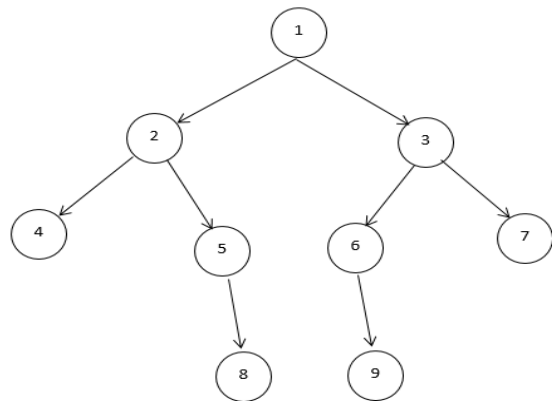


Figure 5- Input Bits in DFS Pattern

Applying Interleaving on this DFS pattern and interleaved results in BFS Pattern.

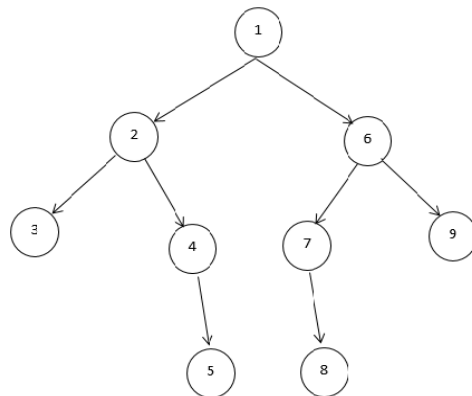


Figure 6- Output Interleaved bit in BFS Pattern

Output Interleaved bits

$D_i = \{1, 2, 6, 3, 4, 7, 9, 5, 8\}$ -----(9)

Equation 9 shows the interleaved bits without burst error. Here burst error is strongly removed as compared with previous technique.

3. CONCLUSION

Instead of using old traditional technique algorithm for designing interleaver for reducing burst error there can use Modern Artificial Intelligence based Algorithms. Which removes burst error very efficiently without affecting the performance of overall system. From the equation-8 and 9 it is clear that MDAIB technique removes burst error strongly as compared with MBAID technique.

4. FUTURE SCOPE

Our main goal is to design interleaver in very efficient way that removes burst error. In this work we have taken the data of 9 bit. In future we can make it for 16-bit, 64-bit, 1024-bit any number of bit. And based upon designing of interleaver in such a way we can also design Deinterleaver. In future we can also design this interleaver on FPGA board and can tested with different IO standards and after analyzing the power consumption we can determine on which IO standard it can design on FPGA with lower power consumption.

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